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EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	8

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/716,493	LAURENTI ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-16* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Extension of Time as received on 2/3/2004 and Amendment A as received on 2/3/2004.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in France on March 10, 2000. It is noted, however, that applicant has not filed a certified copy of the Application No. 00400687.0 as required by 35 U.S.C. 119(b).

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Response to Arguments

6. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection. See below.

Claim Objections

7. Claim 13 is objected to because of the following informalities:

a. Regarding claim 13, the language recites, "and inhibits a fetch of an operand" on its third line. Please correct the claim language to read, "and inhibiting a fetch of an operand" so the language reads more clearly.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1 and 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Regarding claim 1, the claim recites the limitation, "the modification tracking circuitry operable to inhibit a redundant fetch of the operand" on its ninth line. It is unclear from the claim language whether this is a conditional inhibition of a fetch, as described on pgs.22-24 of the specification and in claim 9, or an unconditional inhibition of fetching. If it is the latter, the limitation would render the invention inoperable, as the processor could not run without

instructions being fetched for it to execute, as well as the specification not having antecedent basis for an unconditional inhibition of fetching. Please correct the claim language to more clearly define the metes and bounds of the invention. For the purposes of this examination, the examiner will assume that the limitation refers to a conditional inhibition of fetching.

11. Regarding claim 3, the claim recites, "a stand alone coefficient data pointer" on its second line. It is unclear what the limitation "stand alone" implies that the coefficient data pointer is separate from. For the purposes of this examination, the examiner will assume that "stand alone" refers to this data pointer being physically separate from other circuitry of claim 1, namely the memory interface circuitry that is in communication with the address pointer circuitry.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

13. Claims 1-3 and 9-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Widigen et al., U.S. Patent No. 5,919,256.

14. Regarding claim 1, Widigen has taught a digital system comprising a microprocessor (see Fig.1), wherein the microprocessor comprises:

a. An execution unit (103 of Fig.1),

b. Memory interface circuitry (105 of Fig.1) operable to fetch an operand from memory and to provide the operand to the execution unit (see Col.8 lines 7-16),

c. Address pointer circuitry (102 of Fig.1) operable to provide an address of the operand to the memory interface circuitry (see Col.8 lines 7-16),

d. Modification tracking circuitry connected to the address pointer circuitry, the modification circuitry operable to inhibit a redundant fetch of the operand (see Col.8 lines 7-27). Here, if the operand is not in the operand cache, the operand has to be fetched from memory (see Col.8 lines 7-16), but if the operand is in the operand cache, that operand is sent to the execution unit (see Col.8 lines 19-27), thereby inhibiting a redundant fetch from memory of an operand already located in the operand cache.

15. Regarding claim 2, Widigen has taught the digital system of claim 1, further comprising a shadow register (121 of Fig.1) to hold the operand prior to use by the execution unit (see Col.8 lines 24-27).

16. Regarding claim 3, Widigen has taught the digital system of claim 1, wherein the address pointer circuitry is a stand-alone coefficient data pointer (see Col.4 lines 33-36 and Col.8 lines 7-27). Here, the operand address (pointer) is stored in the address preparation unit, which is separate from the memory interface circuitry (see Fig.1 and above paragraph 11).

17. Regarding claim 9, Widigen has taught a method of operating a digital system comprising a microprocessor, comprising the steps of:

a. Loading a data pointer with a first address value (see Col.8 lines 7-16),

b. Executing a first instruction in the microprocessor that requires at least a first operand from memory in accordance with the data pointer by fetching the first operand from memory in accordance with the first address value (see Col.8 lines 3-16),

c. Executing a second instruction in the microprocessor that requires at least a second operand from memory in accordance with the data pointer by inhibiting fetching of the second operand from memory if the data pointer has not been modified since the step of executing the first instruction (see Col.8 lines 3-27). Here, if the operand address has not changed, the operand of the first instruction will have been fetched from the operand cache, as following the first instructions execution it was fetched and subsequently cached (see Col.8 lines 19-27). This therefore inhibits a redundant fetch from memory of an operand already located in the operand cache.

18. Regarding claim 10, Widigen has taught the method of claim 9, wherein the step of executing the first instruction comprises loading the first operand in to a non-accessible shadow register (104 of Fig.1), such that during the step of executing the second instruction the shadow register is not reloaded if the data pointer has not been modified since the step of executing the first instruction (see Col.8 lines 3-27). Here, if the operand address has not changed, the operand of the first instruction will have been fetched from the operand cache, as following the first instructions execution it was fetched and subsequently cached (see Col.8 lines 19-27). This therefore inhibits a redundant fetch from memory of an operand already located in the operand cache, thus not reloading the operand in the operand cache.

19. Regarding claim 11, Widigen has taught the method of claim 9, further comprising the step of:

a. Loading the data pointer with a second address value between the step of executing the first instruction and the step of executing the second instruction (see Col.8 lines 3-16), and

b. Wherein the step of executing the second instruction comprises fetching the second operand from memory in accordance with the second address value (see Col.8 lines 3-27). Here, because the operand address has changed, the operand pointed to by the updated operand address will be fetched from memory if it is not already located in the operand cache (see Col.8 lines 3-27).

20. Regarding claim 12, Widigen has taught the digital system of claim 1, wherein the address pointer circuitry comprises:

a. A pointer register (401 of Fig.4) for storing at least a portion of a memory address of the operand (see Col.8 lines 27-31 and Col.12 lines 8-23).

b. Wherein the memory interface circuitry fetches operands from memory using the contents of the pointer register for at least a portion of the memory address (see Col.8 lines 9-16). Here, the same address which is stored in the register (401 of Fig.4) in the address preparation circuitry (102 of Fig.1) is the address which is used to fetch the operand from memory (see Col.8 lines 9-16).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 4 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Widigen et al., U.S. Patent No. 5,919,256 as applied to claims 1 and 12 above, and further in view of Touriguian et al., U.S. Patent No. 5,832,257.

23. Regarding claims 4 and 14, taking claim 4 as exemplary, Widigen has taught the digital system of claim 1, wherein the execution unit is used to execute data or address manipulations required by instructions (see Col.4 lines 16-23), but has not explicitly taught wherein the execution unit is a multiply-accumulate (MAC) unit.

24. However, Touriguian has taught that digital signal processors conventionally include at least one multiply-accumulate unit because many digital signal processing applications use the operations multiply and accumulated on sets of data, and having execution units dedicated to these functions can perform them more efficiently than could a general purpose execution unit (see Col.1 lines 11-18). Therefore, one of ordinary skill in the art would have found it obvious to modify the execution unit of the processor of Widigen to be a multiply-accumulate unit so that digital signal processing applications could be executed more efficiently.

25. Claim 14 is nearly identical to claim 4, differing in its parent claim, but encompassing the same scope. Therefore, claim 14 is rejected for the same reasons as claim 4.

26. Regarding claims 15 and 16, taking claim 15 as exemplary, Widigen has taught the digital system of claim 12, wherein the execution units are used to execute data or address manipulations required by instructions (see Col.4 lines 16-23), but has not explicitly taught wherein the execution units comprise a plurality of multiply-accumulate (MAC) units.

27. However, Touriguian has taught that digital signal processors conventionally include at least one multiply-accumulate unit because many digital signal processing applications use the operations multiply and accumulated on sets of data, and having execution units dedicated to these functions can perform them more efficiently than could a general purpose execution unit (see Col.1 lines 11-18). Therefore, one of ordinary skill in the art would have found it obvious to modify the execution units of the processor of Widigen to be multiply-accumulate units so that digital signal processing applications could be executed more efficiently.

28. Claim 16 is nearly identical to claim 15, differing in its parent claim, but encompassing the same scope. Therefore, claim 16 is rejected for the same reasons as claim 15.

29. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widigen et al., U.S. Patent No. 5,919,256 as applied to claim 1 above, and further in view of Schacham et al, UK Patent Application GB2200481A.

30. Regarding claim 5, Widigen has taught the digital system of claim 1, wherein coherency between the operand cache and memory is maintained (see Col.9 lines46-50), but has not explicitly taught wherein a touch instruction "mar(*CDP)" is provided to flag that the operand has been updated in the memory circuit so that the updated operand can be fetched for use by the execution circuit.

31. However, Schacham has taught a cache invalidation instruction which can be executed to invalidate a cache so that operands are forced to be re-fetched (see p.4 lines 28-32). One of ordinary skill in the art would have recognized that for the best performance and correct operation, a cache must contain the most up-to-date information in relation to the main memory (see p.2 lines 8-23), and that ensuring that the correct data is in the cache can be implemented in hardware or by the user in software. Furthermore, there can be problems such as extra hardware needed and address bus contention on the cache if the implementation is carried out in hardware (see p.3 lines 1-13). Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to modify the processor of Widigen to use a cache invalidate instruction to invalidate operands in the operand cache, thereby forcing their re-fetching and ensuring the correct data is available for execution.

32. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widigen et al., U.S. Patent No. 5,919,256 as applied to claim 1 above, and further in view of Okabayashi et al, U.S. Patent No. 6,505,309.

33. Regarding claim 6, Widigen has taught the digital system of claim 1, but has not explicitly taught wherein an override mechanism is provided to disable the modification tracking circuitry.

34. However, Okabayashi has taught the disabling of cache circuitry during a debugging process in order to test if correct sequences of instructions are executed (see Col.1 lines 19-34). One of ordinary skill in the art would have recognized that it is desirable to be able to debug the execution of instructions in a processor separately from the memory and caching systems so that problems can be more accurately located. Therefore, one of ordinary skill in the art at the time

of the invention would have found it obvious to modify the processor of Widigen to provide a mechanism to disable the cache for debugging purposes.

35. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widigen et al., U.S. Patent No. 5,919,256 as applied to claim 1 above, and further in view of Salem et al., U.S. Patent No. 5,623,615.

36. Regarding claim 7, Widigen has taught the digital system of claim 1, but has not explicitly taught wherein the modification tracking circuitry is operable to only track address pointer modification during looping operations of the microprocessor.

37. However, Salem has taught the inhibition of fetching to a cache from memory during loop operations so that power can be saved by not performing redundant fetches (see Col.3 lines 26-47 and Col.14 lines 42-48). Because the modification tracking circuitry is operable when it is inhibiting redundant fetches (see above paragraph 14), one of ordinary skill in the art would have found it obvious to modify the processor of Widigen to inhibit the fetching from memory to a cache during looping operations so that power can be saved by not performing redundant fetches.

38. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widigen et al., U.S. Patent No. 5,919,256 as applied to claim 1 above, and further in view of Willkie et al., U.S. Patent No. 5,923,705.

39. Regarding claim 8, Widigen has taught the digital system according to claim 1, but has not explicitly taught it being cellular telephone.

40. However, Wilkie has taught a cellular telephone, further comprising:

a. An integrated keyboard connected to the processor via a keyboard adapter (see Fig.1),

b. A display, connected to the processor via a display adapter (see Fig.1),

c. Radio frequency (RF) circuitry connected to the processor (see Fig.2), and

d. An aerial connected to the RF circuitry (see Fig.1).

41. One of ordinary skill in the art would have recognized that modern cellular phones require a processor to process digital data and voice signals that are received and transmitted from the phones (see Willkie Col.1 lines 15-20 and 28-31). Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to use the processor (Favor, 10 of Fig.1) in a cellular telephone digital system to process digital data and voice signals.

Allowable Subject Matter

42. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record has taught the limitations of claims 1 and 12, of which claim 13 is dependent upon, specifically circuitry operable to fetch an operand from a memory, and inhibit a redundant fetch of that operand from memory. However, the prior art of record has not taught these parent limitations further comprising circuitry that detects and tracks modifications to the memory address of the operand and subsequently inhibits a redundant fetch if no modifications to that memory address are made.

Conclusion

43. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the

patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
3/23/2004

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